What is claimed is:

1.    A circuit for improving a phase lock of a timing signal for a receiver, comprising:

a sample and hold circuit adapted to receive and hold a phase signal that represents a signal from a phase detector of the receiver;

a switch connected to the sample and hold circuit and adapted to controllably pass the phase signal from the sample and hold circuit for use in adjusting the timing signal for the receiver; and

a decision logic module operably connected to the switch, wherein the decision logic module is adapted to:

detect good signal transitions; and

actuate the switch for good signal transitions such that the phase signal is passed from the sample and hold circuit for use in adjusting the timing signal for the receiver.

2.    The circuit of claim 1, wherein the decision logic module is adapted to detect signal transitions that have zero crossings that deviate from a phase sampling time less than zero crossings for other signal transitions.

3.    The circuit of claim 1, wherein:

the decision logic module includes an input adapted to receive slicer output signals;

the decision logic module is adapted to detect good signal transitions based on the slicer output signals;

the slicer output signals provide logic values for at least two bits; and

the decision logic module is adapted to detect signal transitions between logic values that toggles each of the at least two bits.

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4. The circuit of claim 1, wherein:

the decision logic module includes an input adapted to receive slicer output signals;

the decision logic module is adapted to detect good signal transitions based on the slicer output signals;

the slicer output provides a logic value for a first bit $b_0$ and a second bit $b_1$;

the decision logic module includes:

flip-flop circuitry for holding logic values from the slicer output signals for a first symbol and a successive second symbol, wherein $b_0^0$ and $b_1^0$ represent the first bit and the second bit for the first symbol, and $b_0^1$ and $b_1^1$ represent the first bit and the second bit for the second symbol; and

logic circuitry connected to the flip-flop circuitry and adapted to provide an output Y to actuate the switch to pass the phase signal from the sample and hold circuit for use in adjusting the timing signal for the receiver, wherein

$$Y = \left[ b_0^0 \oplus b_0^1 \right] \cdot \left[ b_1^0 \oplus b_1^1 \right].$$

5. The circuit of claim 1, further comprising a sampling switch connected to the sample and hold circuit, the sampling switch being adapted to controllably pass the phase signal to the sample and hold circuit, wherein the timing signal for the receiver controllably actuates the sampling switch to pass the phase signal to the sample and hold circuit.

6. A receiver for receiving signals from a transmission channel, comprising:

slicer circuitry adapted to receive a signal transmitted through the transmission channel and determine amplitude levels for symbols in the received signal; and

phase locked loop circuitry adapted to:

provide a timing signal for use by the slicer circuitry in determining the amplitude levels for symbols;

detect a phase of the received signal using signal transitions within the received signal;

determine whether the signal transitions are good signal transitions for detecting the phase of the received signal; and

adjust a phase of the timing signal using the good signal transitions.

7. The receiver of claim 6, wherein the slicer circuitry is adapted to receive pulse amplitude modulated (PAM) signals for at least four amplitude levels.

8. The receiver of claim 6, wherein the phase locked loop circuitry includes a decision logic module adapted to determine whether the amplitude levels determined by the slicer circuitry represent good signal transitions for detecting the phase of the received signals.

9. The receiver of claim 6, wherein the decision logic module is adapted to detect signal transitions that have zero crossings that deviate from a phase sampling time less than zero crossings for other signal transitions.

10. The receiver of claim 6, wherein:

the amplitude levels from the received signals represent logic values for at least two bits; and

the decision logic module is adapted to detect signal transitions between logic values that toggles each of the at least two bits.

11. The receiver of claim 10, wherein:

the amplitude levels determined by the slicer circuitry represent a logic value for a first bit $b_0$ and a second bit $b_1$;

the decision logic module includes:

flip-flop circuitry for holding logic values for a first symbol and a successive second symbol, wherein $b_0^0$ and $b_1^0$ represent the first bit and the second bit for the first symbol, and $b_0^1$ and $b_1^1$ represent the first bit and the second bit for the second symbol; and

logic circuitry connected to the flip-flop circuitry and adapted to provide an output Y to be used to adjust a phase of the timing signal using the good signal transitions, wherein

$$Y = \left[b_0^0 \oplus b_0^1\right] \cdot \left[b_1^0 \oplus b_1^1\right].$$

12. The receiver of claim 6, wherein the phase locked loop circuitry includes a decision feedback equalizer, including:

a sample and hold circuit adapted to receive and hold a phase signal that represents the phase of the received signal; and

a switch connected to the sample and hold circuit and adapted to controllably pass the phase signal for good signal transitions from the sample and hold circuit for use in adjusting the phase of the timing signal.

13. A receiver for receiving signals transmitted through a transmission channel, comprising:

slicer circuitry adapted to determine amplitude levels for symbols within a received signal, the slicer circuitry including a slicer output for providing the amplitude levels for the symbols; and

phase locked loop circuitry, including:

a voltage controlled oscillator adapted to provide a timing signal for the slicer circuitry to determine the amplitude levels;

a phase detector adapted to detect signal transitions and provide a phase signal that represents a signal phase for the received signal;

a decision logic module connected to the slicer output and adapted to provide a decision feedback output that indicates whether the amplitude levels represent good signal transitions for detecting the phase of the received signal; and

a decision feedback equalizer adapted to receive the decision feedback output, and pass the phase signal for a good signal transition such that only good signal transitions are used by the voltage controlled oscillator in adjusting the timing signal for the slicer circuitry.

14. The receiver of claim 13, wherein the slicer circuitry is adapted to receive pulse amplitude modulated (PAM) signals for at least four amplitude levels.

15. The receiver of claim 13, wherein the decision logic module includes:

flip-flop circuitry for holding logic values for a first symbol and a successive second symbol, wherein $b_0^0$ and $b_1^0$ represent a first bit and a second bit for the first

symbol, and $b_0^1$ and $b_1^1$ represent a first bit and a second bit for the second symbol; and

logic circuitry connected to the flip-flop circuitry and adapted to provide an output Y to be used to adjust a phase of the timing signal using the good signal transitions, wherein $Y = \left[b_0^0 \oplus b_0^1\right] \cdot \left[b_1^0 \oplus b_1^1\right]$.

16.     The receiver of claim 13, wherein decision feedback equalizer includes:

a sample and hold circuit adapted to receive and hold a phase signal that represents the phase of the received signal; and

a switch connected to the sample and hold circuit and adapted to controllably pass the phase signal for good signal transitions from the sample and hold circuit for use in adjusting the phase of the timing signal.

17.     A method for selecting desirable signal transitions for use in correcting a timing signal for a receiver, comprising:

receiving a signal from a transmission channel, wherein the received signal has symbol pulses with predetermined amplitude levels and signal transitions occur between successive symbol pulses;

determining whether a signal transition is a good transition for determining a phase of the received signal and correcting the timing signal for the receiver;

upon determining that the signal transition is a good transition, adjusting the timing signal for the receiver using the good transition.

18.     The method of claim 17, wherein determining whether a signal transition is a good transition includes determining whether the transition from a first amplitude level to a second amplitude level is symmetrical about a zero-crossing.

19.     The method of claim 17, wherein:

each of the symbol pulses includes a logic value for N bits in a pulse amplitude modulated system; and

determining whether a signal transition is a good transition includes determining whether each of the N bits has been toggled during the transition.

20.     The method of claim 17, wherein:

each of the symbol pulses includes a logic value for a first bit and a second bit in a pulse amplitude modulated system;

$b_0^0$ and $b_1^0$ represent the first bit and the second bit for a first symbol pulse;

$b_0^1$ and $b_1^1$ represent the first bit and the second bit for a second symbol pulse;

determining whether a signal transition is a good transition includes determining whether a logic output Y is 1, wherein $Y = \left[ b_0^0 \oplus b_0^1 \right] \cdot \left[ b_1^0 \oplus b_1^1 \right]$.

21.     A method for selecting desirable signal transitions for use in correcting a timing signal for a receiver, comprising:

receiving a first symbol pulse and a second symbol pulse from a transmission channel, wherein the first symbol pulse and the second symbol pulse have amplitude levels, and wherein a signal transition occurs between the first symbol pulse and the second symbol pulse;

detecting a signal phase for one of the first symbol pulse and the second symbol pulse using the signal transition and the timing signal for the receiver;

sampling a signal that represents the signal phase using the timing signal for the receiver;

determining amplitude levels for the first symbol pulse and the second symbol pulse;

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determining whether the signal transition between the amplitude levels for the first and second symbol pulses is a good transition for determining the signal phase and correcting the timing signal for the receiver; and

upon determining that the signal transition is a good transition, passing the sampled signal that represents the signal phase to a loop filter and a voltage controlled oscillator for use in adjusting the timing signal for the receiver.

22. The method of claim 21, wherein determining whether the signal transition between the amplitude levels for the first and second symbol pulses is a good transition includes determining whether the signal transition for the detected signal phase has a zero crossing near a phase sampling time that is controlled by the timing signal for the receiver.

23. The method of claim 21, wherein determining whether the signal transition between the amplitude levels for the first and second symbol pulses is a good transition includes determining whether the signal transition is symmetrical about a zero-crossing.

24. The method of claim 21, wherein:

each of the first and second received symbol pulses includes a logic value for N bits in a pulse amplitude modulated system; and

determining whether the signal transition between the amplitude levels for the first and second signals is a good transition includes determining whether each of the N bits has been toggled during the transition.

25. The method of claim 21, wherein:

each of the first and second received symbol pulses include a logic value for 2 bits in a pulse amplitude modulated system;

$b_0^0$ and $b_1^0$ represent the first bit and the second bit for a first symbol pulse;

$b_0^1$ and $b_1^1$ represent the first bit and the second bit for the second symbol pulse;

determining whether the signal transition between the amplitude levels for the first and second symbol pulses is a good transition includes determining whether a logic output Y is 1, wherein $Y = \left[ b_0^0 \oplus b_0^1 \right] \cdot \left[ b_1^0 \oplus b_1^1 \right]$.

26.    The method of claim 21, wherein passing the sampled signal includes actuating a switch to pass the sampled signal from a sample and hold circuit to the loop filter and the voltage controlled oscillator using a decision feedback signal that indicates that the signal transition between the amplitude levels for the first and second symbol pulses is a good transition.